Exhibit D-1

United States Patent Office

3,290,446

Patented Dec. 6, 1966

3,290,446

REGISTER POSITION IN A MULTI-STAGE SWITCHING NETWORK

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Filed Aug. 13, 1963, Ser. No. 302,232
3 Claims. (Cl. 179—18)

This invention relates to multi-stage switching networks and more particularly to the positioning of registers within such networks.

The principal object of this invention is to provide a novel placement of registers in a multi-stage switching network to improve the traffic handling capability of the system.

In a multi-stage switching network registers must be provided to accept the address information so that connections can be set up within the network. These registers must be available to all lines and should be located within the network so that: (1) they can be easily connected to lines, (2) they contribute little to the blocking characteristics of the system, and (3) the chances of a line being blocked from a register are minimum. The novel approach to placement of registers according to this invention is to provide a register on each secondary switch of a multi-stage switching network.

An advantage of the novel register placement of this invention is that lines connecting to registers tie up only one idle link. Since the number of links per rectangular primary switch equals the number of secondary switches, all lines have a non-blocking access to at least one register regardless of whether line to line type connections are blocking or non-blocking.

These and other objects and advantages of this invention will become more apparent from the following description taken in conjunction with the drawings in which:

FIG. 1 is a diagram showing register position in the multi-stage switching network, and

FIG. 2 shows a block diagram of the major functional blocks used to effect a call.

Referring to FIG. 1, there is shown a matrix consisting of an array of rectangular primary switches and two sets of triangular matrices. The overall matrix is divided into sections labeled PRIMARY STAGE, which consists of four primary switches PS1 to PS4, and SECONDARY STAGE, which consists of five secondary switches SS1 to SS5.

Each primary switch consists of a triangular matrix, which is defined by the intersection of verticals V1 to V5 and horizontals H6 to H9, and a rectangular matrix which is defined by the intersection of verticals V1 to V5 and horizontals H1 to H5. Each secondary switch consists of a triangular matrix which comprises verticals V1 to V4 and horizontals H1 to H5. The horizontals H1 to H4 of each secondary switch are respectively coupled to one of the horizonals on each of the primary switches. For example, horizontal H1 of secondary switch SS1 is connected to horizontal H1 of primary switch PS1, horizontal H2 of switch SS1 is connected to horizontal H1 of switch PS2, and so on. Similiarly, horizontal H1 of switch SS2 is connected to horizontal H2 of switch PS1, horizontal H2 of switch SS2 is connected to horizontal H2 of switch PS2, and so on. In this manner, each primary switch is connected to each of the remaining primary switches through each of the secondary switches. Horizontal H5 on each secondary switch is connected to a register, horizontal H5 on switches SS1 to SS5 being connected to registers 11 to 15 respectively. In this

type of array all lines, trunks, operators, registers, or any inputs or outputs appear as verticals on the primary switches and are interchangeable.

A connection between two lines on the same primary switch is accomplished by closing a crosspoint on the primary switch triangular matrix. Thus, if verticals V3 and V5 of switch PS2 are to be connected, the crosspoint at the intersection of vertical V5 and horizontal H7 is closed. A connection between two lines on different primary switches is accomplished by closing one crosspoint on the respective primary switch rectangular matrices and one crosspoint on the interconnecting secondary triangular switch. A typical connection of this type would be between vertical V1 of switch PS1 and vertical V3 of switch PS3. To complete such a connection, the crosspoints could be closed at the intersections of vertical V1 and horizontal H2 of switch PS1, vertical V1 and horizontal H3 of switch SS2 and vertical V3 and horizontal H2 of switch PS3. It is obvious that the connection between these two terminals could be made through any of the secondary switches unless one or more of the links involved was already in use, whereupon the number of available connecting routes would decrease.

Registers 11 to 15 are provided to accept address information in order to set up connections within the switching network. These registers must be available to all lines and trunks. Registers could be made to appear as lines on primary switches as shown by dashed lines as vertical V1 on switch PS3. This method would require two idle links in order to connect a line on a different primary switch to the register. These links are made busy during this connection and are therefore not available for line to line type connections.

The novel approach, which is the subject matter of this invention, provides a register on each of the secondary switches SS1 to SS5. With the registers on secondary switches, lines connecting to registers tie up only one idle link. Thus all lines have a non-blocking access to at least one register, regardless of whether line to line type connections are blocking or non-blocking. For example, if horizontals H1 to H4 of primary switch PS1 were in use, a vertical such as V1 would still have access to register 15 through horizontal H5.

In order to illustrate the relationship of the registers to the switching matrix and the remaining control circuitry of the system, a typical call will be traced through the switchboard. FIG. 2 shows the major functional blocks used to effect the call. For the sake of simplicity, the switching matrix is shown as having a reduced number of switches per stage and a reduced number of verticals and horizonals per switch. Line circuits 31 to 34 and trunk circuits 35 and 36 are connected to the six verticals shown in FIG. 2 as constituting the primary stage. Registers 37 and 38 are connected to one of the horizontals in each of the two secondary switches, respectively, which make up the secondary stage. Incorporated in each of the line and trunk circuits is a memory, the function of which will be hereinafter explained. A plurality of blocks are grouped together within a block labeled common control. The functions of the common control circuits are to scan all lines for calling party order signals (seizure, recall, and release), to sequentially serve all lines and trunks, to sequentially serve all registers, and to activate matrix crosspoints.

This system is characterized by its synchronous and sequential mode of operation. Each operation is alloted a time slot in which a function is carried out. This in effect eliminates any interference between functions and facilitates trouble shooting and self verifica-